REMARKS

In the final Office Action, the Examiner rejected claims 1-8 and 17-27 under 35 U.S.C. § 102(e) as anticipated by Jaramillo et al. (U.S. Patent No. 6,598,104); and rejected claims 9-16 and 28-31 under 35 U.S.C. § 102(e) as anticipated by Cranston et al. (U.S. Patent No. 6,253,269).

By this Amendment, Applicant proposes canceling claims 29-31 without prejudice or disclaimer and amending claims 1 and 28 to improve form. Applicant traverses the Examiner's rejection under 35 U.S.C. § 102 with regard to the claims as now amended. Claims 1-28 will be pending after entry of this amendment.

At the outset, Applicant respectfully submits that the finality of the Office Action, dated June 4, 2004, is improper. In the previous Office Action, dated January 2, 2004, the Examiner rejected claims 1-31 under 35 U.S.C. § 102(e) as anticipated by Smith (U.S. Patent No. 6,629,178). Applicant subsequently filed an Amendment on March 18, 2004 with a minor change to independent claim 27 and no change to independent claim 28. In the final Office Action, dated June 4, 2004, the Examiner newly rejected claim 27 under 35 U.S.C. § 102(e) as anticipated by Jaramillo et al. and newly rejected claim 28 under 35 U.S.C. § 102(e) as anticipated by Cranston et al. The Examiner made the rejection final, alleging that Applicant's amendment necessitated the new grounds of rejection (final Office Action, page 10).

M.P.E.P. § 706.07(a) states that "second or any subsequent actions on the merits shall be final, except where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p)." The change Applicant made to claim 27 in the previously filed Amendment

could not have necessitated the Examiner's application of a new ground of rejection. In addition, independent claim 28 was not amended in the previously filed Amendment. Further, neither the Jaramillo et al. reference nor the Cranston et al. reference was cited by Applicant in an Information Disclosure Statement filed during the period set forth in 37 CFR 1.97(c). Accordingly, Applicant submits that the finality of the Office Action, dated June 4, 2004, is improper. Withdrawal of the finality of the Office Action, dated June 4, 2004, is, therefore, respectfully requested.

In paragraph 2 of the final Office Action, the Examiner rejected claims 1-8 and 17-27 as allegedly anticipated by Jaramillo et al. Applicant respectfully traverses the rejection.

Amended independent claim 1, for example, recites a combination of features of a system for selecting bus mastership in a multi-master system. The system includes a plurality of master devices and a plurality of slave devices connected to the master devices via a bus. The master devices are configured to generate control signals relating to control of the bus in the multi-master system. Each of the slave devices is configured to receive the control signals from the master devices, determine whether a conflict in the control signals exists, generate one or more alternate control signals for selecting bus mastership when a conflict is determined to exist, and determine which of the master devices obtains control of the bus using the one or more alternate control signals when a conflict is determined to exist.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either expressly or impliedly. Any feature not directly taught must be inherently present. In other words, the identical invention must be shown in as complete detail as contained in the claim. See M.P.E.P. § 2131. Jaramillo et al. does not disclose or

suggest the combination of features recited in amended claim 1. For example, Jaramillo et al. does not disclose or suggest a plurality of slave devices connected to a plurality of master devices via a bus, where each slave device is configured to receive control signals from the master devices, determine whether a conflict in the control signals exists, generate one or more alternate control signals for selecting bus mastership when a conflict is determined to exist, and determine which of the master devices obtains control of the bus using the one or more alternate control signals when a conflict is determined to exist.

The Examiner appears to allege that PCI initiators 402-404 correspond to the plurality of master devices recited in claim 1 and PCI target agent 405 corresponds to the plurality of slave devices recited in claim 1 (final Office Action, pages 2-3). The Examiner alleged that Jaramillo et al. discloses the features of claim 1 and cited column 4, lines 33-37, column 5, lines 52-62, and column 5, line 52 - column 6, line 40, of Jaramillo et al. for support (final Office Action, pages 2-3). Applicant respectfully disagrees.

At column 4, lines 33-37, Jaramillo et al. discloses:

> In one embodiment, the present invention comprises a smart retry system for a device in a computer system. The smart retry system of the present invention includes a master device, a slave device, an arbiter, and a smart retry logic component, all adapted to be coupled to a bus.

Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest a slave device that, for example, is configured to determine whether a conflict exists in control signals received from master devices that relate to control of a bus or determine which of the master devices obtains control of the bus using one or more alternate control signals when a conflict is determined to exist, as recited in claim 1.

At column 5, line 52 - column 6, line 40, Jaramillo et al. discloses:

FIG. 3 shows a block diagram of a smart retry access process 300 utilized in accordance with one embodiment of the present invention. On the left side of process 300 in step 301, a PCI initiator agent accesses a PCI target agent and attempts a data transmission. The initial access is comprised of the normal stages of a PCI transaction (e.g., arbitration for PCI bus ownership, receiving a grant signal from a PCI arbiter, addressing and informing a PCI target agent of the data to be transferred, etc.). In step 302 the PCI target agent issues a retry in instances where the PCI target agent is busy and cannot complete the data transaction.

In step 303, in accordance with the present embodiment, the PCI target agent issues a first signal or bus denial signal, that indicates the smart retry system should deny PCI bus access to the PCI initiator agent. Denying the PCI initiator agent PCI bus access permits the PCI bus to be available for use by other PCI initiator agents. Thus, in step 304 the PCI initiator agent repeatedly attempts to access the PCI bus but is not granted access. In so doing, the smart retry system of the present invention minimizes wasted time associated with futile retry attempts. That is, unlike prior art, the present embodiment prevents the PCI initiator from arbitrating for PCI bus ownership, receiving a grant signal, addressing and attempting to access the PCI target agent. Hence, all of that "wasted" PCI bus time is eliminated by the present embodiment.

In step 305, when the PCI target agent is no longer busy it signals the PCI arbiter to grant PCI bus access to the PCI initiator agent. In step 306 the PCI initiator agent retries and is finally granted PCI bus access. In step 307 the PCI initiator agent successfully accesses the PCI target agent and completes a data transmission.

It should be appreciated that the present embodiment relies on a PCI initiator agent attempting to access only one PCI target agent at a time. It should be further appreciated that in the preferred embodiment, when a PCI target agent issues a retry, the PCI initiator agent repeatedly requests the PCI bus for purposes of accessing the same PCI target agent. The PCI initiator agent does this until it completes a transaction with the PCI target agent that issued the retry, before attempting to access any other PCI target agents. PCI systems typically behave in this manner. That is, if a retry is issued the PCI initiator agent continually retries to access the same PCI target agent before attempting to access any other PCI target agents.

It should be appreciated the present invention can be adapted by one skilled in the art to accommodate other configurations of a PCI system. For example, when a PCI target agent signals a PCI initiator agent to retry later, the PCI initiator agent can access the PCI bus for purposes of communicating with other PCI target agents. However, unless the PCI target agent is ready, the PCI initiator agent can not access the PCI bus for purposes of communicating with the PCI target agent that issued the retry.

In this section, a PCI initiator agent (which the Examiner alleged was equivalent to a master device) attempts to gain bus ownership to perform a data transaction with a PCI target agent (which the Examiner alleged was equivalent to a slave device) and the PCI target agent issues a retry when the PCI target agent is busy and cannot complete the data transaction. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest a slave device that is configured to determine whether a conflict exists in control signals received from master devices that relate to control of a bus or determine which of the master devices obtains control of the bus using one or more alternate control signals when a conflict is determined to exist, as recited in claim 1.

In other words, Jaramillo et al. does not disclose or suggest that the PCI target agent determines whether a conflict exists in control signals received from the PCI initiator agents that relate to control of a bus. Instead, PCI target agent issues a retry which denies the PCI initiator agent bus access when PCI target agent is busy with an internal activity, engaging in a transaction that would generate a conflict, or will be slowed in completing a transaction (col. 8, lines 57-61). While Jaramillo et al. discloses that a PCI target agent issues a retry when engaging in a transaction that would generate a conflict, Jaramillo et al. does not disclose or suggest determining whether a conflict exists in control signals received from master devices that relate to control of a bus, as required by claim 1. Further, Jaramillo et al. discloses that denying the PCI initiator agent bus access permits the PCI bus to be available for use by other PCI initiator agents (col. 5, line 66 - col. 6, line 1). Therefore, any conflict in the PCI target agent has nothing to do with a conflict in control signals from master devices that relate to control of the bus.

Jaramillo et al. also does not disclose or suggest a slave device that is configured to determine which of the master devices obtains control of the bus using one or more alternate control signals generated when a conflict is determined to exist, as required by claim 1. As explained above, Jaramillo et al. does not disclose that the PCI target agent determines whether a conflict exists in control signals from PCI initiator agents that relate to control of a bus. Therefore, Jaramillo et al. cannot disclose that the PCI target agent determines which of the PCI initiator agents obtains control of the bus using one or more alternate control signals that are generated when a conflict is determined to exist.

For at least these reasons, Applicant submits that claim 1 is not anticipated by Jaramillo et al. Claims 2-7 depend from claim 1 and are, therefore, not anticipated by Jaramillo et al. for at least the reasons given with regard to claim 1. Claims 2-7 are also not anticipated by Jaramillo et al. for reasons of their own.

For example, claim 2 recites bus selection logic that is configured to determine whether the control signals indicate that two or more of the master devices concurrently assert control of the bus and generate a conflict indication signal when two or more of the master devices concurrently assert control of the bus, and conflict resolution logic that is configured to generate the one or more alternate control signals in response to the conflict indication signal. Jaramillo et al. does not disclose this combination of features. For example, Jaramillo et al. does not disclose or suggest bus selection logic that is configured to determine whether the control signals indicate that two or more of the master devices concurrently assert control of the bus and generate a conflict indication signal when two or more of the master devices concurrently assert control of the bus.

The Examiner alleged that Jaramillo et al. discloses bus selection logic and cited column 5, line 52 - column 6, line 40, of Jaramillo et al. for support (final Office Action, page 3). Applicant disagrees.

Column 5, line 52 - column 6, line 40, of Jaramillo et al. has been reproduced above. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest, for example, determining whether the control signals indicate that two or more of the master devices concurrently assert control of the bus, as recited in claim 2. Instead, Jaramillo et al. discloses that a PCI target agent issues a retry when the PCI target agent is busy and cannot complete a transaction (col. 5, lines 60-62). Jaramillo et al. is concerned with PCI target agent availability and not bus conflicts as evident by the fact that Jaramillo et al. discloses that a PCI initiator agent that has received a retry signal from one PCI target agent can access the bus for purposes of communicating with other PCI target agents (col. 6, lines 33-40).

For at least these additional reasons, Applicant submits that claim 2 is not anticipated by Jaramillo et al.

Claim 3 recites that the one or more alternate control signals include a bus switch signal that indicates whether a change in control of the bus is to occur and a bus select signal that indicates which of the master devices is to be granted control of the bus. Jaramillo et al. does not disclose or suggest this claimed combination of features. For example, Jaramillo et al. does not disclose a bus switch signal that indicates whether a change in control of the bus is to occur.

The Examiner alleged that Jaramillo et al. discloses a bus switch signal and cited column 6, lines 51-67, of Jaramillo et al. for support (final Office Action, page 4). Applicant disagrees.

At column 6, lines 51-67, Jaramillo et al. discloses:

> FIG. 5 shows PCI system 400 with signal and data lines broken out of PCI bus 406. PCI bus 406 comprises the following data and signal lines: request bus req_n (2:0) 501, grant bus gnt_n (2:0) 502, bus_request_mask (2:0) 503, frame_n 504, irdy_n 505, trdy_n 506, stop_n 507 and devsel_n 508. PCI Bus 406 further comprises data and signal lines that have not been shown in detail in FIG. 5 so as not to unnecessarily obscure the current invention. PCI target agent 405 of the present embodiment includes the ability to access a second signal (hereinafter referred to as the PCI bus grant signal) indicating the grant status of the PCI bus 406. It should appreciated that the PCI bus grant signal is communicated via the grant bus gnt_n (2:0) 502 shown in FIG. 5. The grant bus gnt_n (2:0) 502 is snooped by PCI initiator agents 402, 403 and 404 and, in accordance with the present embodiment, the grant bus gnt_n (2:0) 502 is also snooped by PCI target agent 405.

Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest that any of these bus data and signal lines indicates whether a change in control of the bus is to occur. If the Examiner believes differently, Applicant requests that the Examiner specifically identify which of these bus signal lines allegedly corresponds to the claimed bus switch signal.

For at least these additional reasons, Applicant submits that claim 3 is not anticipated by Jaramillo et al.

Claim 4 recites that each of the slave devices comprises bus selection logic configured to determine whether the control signals indicate that none of the master devices asserts control of the bus and maintain a previous grant of control of the bus when none of the master devices asserts control of the bus. Jaramillo et al. does not disclose or suggest this combination of features.

The Examiner alleged that Jaramillo et al. discloses these features and cited column 8, lines 15-35, of Jaramillo et al. for support (final Office Action, page 4). Applicant submits that the section of Jaramillo et al. identified by the Examiner corresponds to PCI arbiter 401 and not a slave device, as required by claim 4. Therefore, regardless of the accuracy of the Examiner's allegation, Jaramillo et al. does not disclose or suggest each of a plurality of slave devices that

comprise bus selection logic configured to determine whether the control signals indicate that none of the master devices asserts control of the bus and maintain a previous grant of control of the bus when none of the master devices asserts control of the bus, as required by claim 4.

For at least these additional reasons, Applicant submits that claim 4 is not anticipated by Jaramillo et al.

Claim 6 recites that the control signals include a present signal that indicates whether a corresponding one of the master devices is operating and a master signal that indicates whether a corresponding one of the master devices asserts control of the bus. Jaramillo et al. does not disclose this combination of features. For example, Jaramillo et al. does not disclose or suggest a present signal that indicates whether a corresponding one of the master devices is operating.

The Examiner alleged that Jaramillo et al. discloses a present signal and cited column 5, line 52 - column 6, line 40, of Jaramillo et al. for support (final Office Action, pages 4-5). Applicant disagrees.

Column 5, line 52 - column 6, line 40, of Jaramillo et al. has been reproduced above. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest anything resembling a present signal that indicates whether a corresponding one of the master devices is operating, as recited in claim 6. If the Examiner believes differently, Applicant respectfully requests that the Examiner specifically identify which signal in Jaramillo et al. allegedly corresponds to the present signal recited in claim 6.

For at least these additional reasons, Applicant submits that claim 6 is not anticipated by Jaramillo et al.

Independent claim 8 recites a combination of features of a system for selecting a master in a multi-master system. The system includes means for outputting first and second control signals relating to mastership in the multi-master system from each of a plurality of masters in the multi-master system, means for determining whether a conflict for mastership exists based on the first and second control signals, means for generating a switch signal and a select signal when a conflict is determined to exist, and means for selecting one of the masters using the switch signal and the select signal.

Jaramillo et al. does not disclose or suggest this claimed combination of features. For example, Jaramillo et al. does not disclose or suggest means for generating a switch signal and a select signal when a conflict for mastership is determined to exist. The Examiner alleged that Jaramillo et al. discloses this feature and cited column 5, line 52 - column 6, line 40, of Jaramillo et al. for support (final Office Action, page 5). Applicant disagrees.

Column 5, line 52 - column 6, line 40, of Jaramillo et al. has been reproduced above. In this section, a PCI initiator agent attempts to gain bus ownership to perform a data transaction with a PCI target agent and the PCI target agent issues a retry when the PCI target agent is busy and cannot complete the data transaction. Nowhere in this section, or elsewhere, does Jaramillo et al. disclose or suggest means for generating a switch signal and a select signal when a conflict for mastership is determined to exist, as recited in claim 8.

For at least these reasons and reasons similar to reasons given above with regard to claim 1, Applicant submits that claim 8 is not anticipated by Jaramillo et al.

Independent claim 17 recites features similar to features recited in claim 8. Claim 17 is, therefore, not anticipated by Jaramillo et al. for reasons similar to reasons given with regard to claim 8.

Independent claim 18 recites features similar to features recited in claim 2. Claim 18 is, therefore, not anticipated by Jaramillo et al. for reasons similar to reasons given with regard to claim 2. Claims 19-22 depend from claim 18 and are, therefore, not anticipated by Jaramillo et al. for at least the reasons given with regard to claim 18. Claims 19-22 also recite features similar to various features recited in claims 3-7. Claims 19-22 are, therefore, also not anticipated by Jaramillo et al. for reasons similar to reasons given with regard to claims 3-7.

Independent claim 23 recites features similar to features recited in claim 18. Claim 23 is, therefore, not anticipated by Jaramillo et al. for reasons similar to reasons given with regard to claim 18. Claims 24-26 depend from claim 23 and are, therefore, not anticipated by Jaramillo et al. for at least the reasons given with regard to claim 23. Claims 24-26 also recite features similar to various features recited in claims 19-22. Claims 24-26 are, therefore, also not anticipated by Jaramillo et al. for reasons similar to reasons given with regard to claims 19-22.

Independent claim 27 recites a combination of features of a multi-master system that includes a plurality of master devices, conflict resolution logic, and a plurality of slave devices. The master devices are configured to generate control signals relating to bus mastership. The conflict resolution logic is configured to receive the control signals from the master devices, determine whether the control signals indicate that two or more of the master devices concurrently assert bus mastership, and generate a switch signal and a select signal when it is determined that two or more of the master devices concurrently assert bus mastership. The slave

devices are configured to select bus mastership using the switch signal and the select signal when the control signals indicate that two or more of the master devices concurrently assert bus mastership.

Jaramillo et al. does not disclose or suggest this claimed combination of features. For example, Jaramillo et al. does not disclose or suggest conflict resolution logic that is configured to, for example, generate a switch signal and a select signal when it is determined that two or more of the master devices concurrently assert bus mastership. The Examiner alleged that Jaramillo et al. discloses these features and cited column 6, lines 18-67, of Jaramillo et al. for support (final Office Action, pages 5-6). Applicant disagrees.

At column 6, lines 18-67, Jaramillo et al. discloses:

> It should be appreciated that the present embodiment relies on a PCI initiator agent attempting to access only one PCI target agent at a time. It should be further appreciated that in the preferred embodiment, when a PCI target agent issues a retry, the PCI initiator agent repeatedly requests the PCI bus for purposes of accessing the same PCI target agent. The PCI initiator agent does this until it completes a transaction with the PCI target agent that issued the retry, before attempting to access any other PCI target agents. PCI systems typically behave in this manner. That is, if a retry is issued the PCI initiator agent continually retries to access the same PCI target agent before attempting to access any other PCI target agents.
>
> It should be appreciated the present invention can be adapted by one skilled in the art to accommodate other configurations of a PCI system. For example, when a PCI target agent signals a PCI initiator agent to retry later, the PCI initiator agent can access the PCI bus for purposes of communicating with other PCI target agents. However, unless the PCI target agent is ready, the PCI initiator agent can not access the PCI bus for purposes of communicating with the PCI target agent that issued the retry.
>
> FIG. 4 shows a general PCI system 400, in accordance with one embodiment of the present invention. PCI system 400 includes the following items all coupled to PCI bus 406: PCI arbiter 401, PCI initiator agent A 402, PCI initiator agent B 403, PCI initiator agent C 404, and PCI target agent 405. So as not to unnecessarily obscure the current invention, only one PCI target agent 405 is shown. However, as discussed below, it should be appreciated that other embodiments of the present invention can be realized in systems comprising a plurality of PCI target agents. PCI bus 406 contains a plurality of communication lines.

> FIG. 5 shows PCI system 400 with signal and data lines broken out of PCI bus 406. PCI bus 406 comprises the following data and signal lines: request bus req_n (2:0) 501, grant bus gnt_n (2:0) 502, bus_request_mask (2:0) 503, frame_n 504, irdy_n 505, trdy_n 506, stop_n 507 and devsel_n 508. PCI Bus 406 further comprises data and signal lines that have not been shown in detail in FIG. 5 so as not to unnecessarily obscure the current invention. PCI target agent 405 of the present embodiment includes the ability to access a second signal (hereinafter referred to as the PCI bus grant signal) indicating the grant status of the PCI bus 406. It should appreciated that the PCI bus grant signal is communicated via the grant bus gnt_n (2:0) 502 shown in FIG. 5. The grant bus gnt_n (2:0) 502 is snooped by PCI initiator agents 402, 403 and 404 and, in accordance with the present embodiment, the grant bus gnt_n (2:0) 502 is also snooped by PCI target agent 405.

Nowhere in this section does Jaramillo et al. disclose the situation where two or more master devices concurrently assert bus mastership. Instead, Jaramillo et al. discloses the situation where a PCI initiator agent attempts to gain bus ownership to perform a data transaction with a PCI target agent and the PCI target agent issues a retry when the PCI target agent is busy and cannot complete the data transaction. Therefore, Jaramillo et al. cannot disclose or suggest generating a switch signal and a select signal when it is determined that two or more of the master devices concurrently assert bus mastership, as recited in claim 27.

Jaramillo et al. also does not disclose or suggest a plurality of slave devices that are configured to select bus mastership using the switch signal and the select signal when the control signals indicate that two or more of the master devices concurrently assert bus mastership, as further recited in claim 27. The Examiner alleged that Jaramillo et al. discloses these features and cited column 6, lines 18-67, of Jaramillo et al. for support (final Office Action, page 6). Applicant disagrees. Because Jaramillo et al. does not disclose a switch signal and a select signal, Jaramillo et al. cannot disclose or suggest a slave device that is configured to select bus

mastership using the switch signal and the select signal when the control signals indicate that two or more of the master devices concurrently assert bus mastership, as recited in claim 27.

For at least these reasons, Applicant submits that claim 27 is not anticipated by Jaramillo et al.

In paragraph 3 of the final Office Action, the Examiner rejected pending claims 9-16 and 28 under 35 U.S.C. § 102(e) as allegedly anticipated by Cranston et al. Applicant respectfully traverses the rejection.

Independent claim 9 recites, for example, a combination of features of a method for selecting a bus in a multi-bus system. The method includes generating control signals relating to bus selection in the multi-bus system, determining whether a conflict for bus selection exists based on the control signals, generating one or more alternate control signals when a conflict is determined to exist, and selecting a bus using the one or more alternate control signals.

Cranston et al. does not disclose or suggest the combination of features recited in claim 9. For example, Cranston et al. does not disclose or suggest generating one or more alternate control signals when a conflict for bus selection is determined to exist. The Examiner alleged that Cranston et al. discloses this feature and cited column 7, lines 17-37, of Cranston et al. for support (final Office Action, page 6). Applicant disagrees.

At column 7, lines 17-37, Cranston et al. discloses:

> It should be understood that the arbiter 50 can use a variety of procedures to select between the plurality of communication buses. FIG. 10 shows a general method that can be utilized by the arbiter 50 to select the appropriate communication bus to interface to the application card 20. At Step 100, the arbiter 50 monitors the plurality of communication buses to determine if a communication buses has become active with data from a management card. At Step 102, an active communication bus can be determined in any variety of ways well known to those skilled in the art including

> monitoring protocols sent on the communication buses.
>
> At Step 104, the active communication bus is allowed access to the application card by connecting or switching the active communication bus to the local bus of the application card. The access to the local card can be provided by a switching function device implemented through an integrated switching matrix, a simple decoder or other solid state integrated circuit. At Step 106, the arbiter prevents the other communication buses from accessing the application card to prevent possible conflicts and contention between the buses.

In this section, Cranston et al. discloses that the arbiter permits access to the application card to an active communication bus and prevents access to other communication buses. Nowhere in this section, or elsewhere, does Cranston et al. disclose that the arbiter generates one or more alternate control signals when a conflict for bus selection is determined to exist, as required by claim 9. If the Examiner believes differently, Applicant requests that the Examiner specifically identify what signal(s) in Cranston et al. allegedly correspond to the one or more alternate control signals recited in claim 9.

Because Cranston et al. does not disclose or suggest generating one or more alternate control signals, Cranston et al. cannot disclose or suggest selecting a bus using the one or more alternate control signals, as further recited in claim 9. The Examiner alleged that Cranston et al. discloses this feature and cited column 7, lines 17-56, of Cranston et al. for support (final Office Action, page 6). Applicant disagrees.

At column 7, lines 17-56, of which lines 17-37 have been reproduced above, Cranston et al. discloses:

> Because the I^2C-bus is bidirectional, the arbiter also preferably includes knowledge of the I^2C protocol to appropriately switch the bus direction as described above.
>
> Alternatively, the arbiter may select among a plurality of communication buses according to a programmed algorithm or other criteria. A priority can be assigned to communication buses and the priority of the communication bus used to selected the

> appropriate communication bus to allow access to the application card. A priority can also be utilized to allow a communication bus to preempt communication buses of lower priority. Communication buses may be assigned to classes in which certain classes are allowed simultaneous access to the application card and other classes of communication buses access the card mutually exclusively. The management card may download updated priority scheme to the arbiter over to the I^2C-bus. Using the arbiter, any arbitrary scheme for selecting among a plurality of communication buses may be implemented and tailored and modified according to the needs of the particular device.

In this section, Cranston et al. discloses that buses may be selected based on the priorities assigned to the buses. Nowhere in this section, or elsewhere, does Cranston et al. disclose that the arbiter generates one or more alternate control signals when a conflict for bus selection is determined to exist or selects a bus using the one or more alternate control signals, as required by claim 9.

For at least these reasons, Applicant submits that claim 9 is not anticipated by Cranston et al. Claims 10-16 depend from claim 9 and are, therefore, not anticipated by Cranston et al. for at least the reasons given with regard to claim 9.

Amended independent claim 28 recites features similar to features recited in claim 9. Claim 28 is, therefore, not anticipated by Cranston et al. for reasons similar to reasons given with regard to claim 9.

In view of the foregoing amendments and remarks, Applicant respectfully requests the Examiner's reconsideration of the application and the timely allowance of pending claims 1-28.

Applicant respectfully requests that the finality of the Office Action be withdrawn as improper for the reasons provided above. Accordingly, this Amendment should be entered by the Examiner, placing claims 1-28 in condition for allowance.

In the event that the Examiner does not withdraw the finality of the Office Action, Applicant respectfully requests that this Amendment under 37 C.F.R. § 1.116 be entered by the

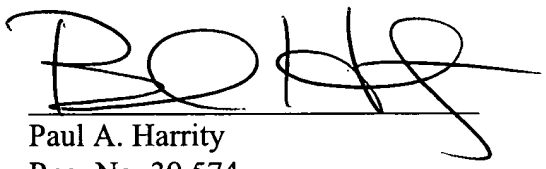
Examiner, placing claims 1-28 in condition for allowance. Applicant submits that the proposed amendments do not raise new issues or necessitate the undertaking of any additional search of the art by the Examiner, since all of the elements and their relationships claimed were either earlier claimed or implied in the claims as examined. Therefore, this Amendment should allow for immediate action by the Examiner.

If the Examiner does not believe that all pending claims are now in condition for allowance, the Examiner is urged to contact the undersigned to expedite prosecution of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY & SNYDER, L.L.P.



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